REMARKS

Claims 1, 17 and 27 have been amended. Claims 1-36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0041650 and Provisional Application No. 60/217,520 to Richmond. Applicant respectfully disagrees.

The Richmond Reference

Richmond is directed to a method that "reduces the complexity of the circuitry...to compensate for drift between the frequencies of the transmit and receive clocks" (paragraph [0008]). For example, Figure 2 shows an elastic buffer 24 that is used to detect overflow or underflow and "resynchronize the receive data to the transmit clock" (paragraph [0021]). The elastic buffer receives a receive clock (via line 26) along with received data (via line 28) and a transmit clock (via line 30), and "serves to insert or delete primitives as needed to compensate for drift between the receive clock and the transmit clock so as to output data on line 34 at the transmit clock rate" ([0021]).

Figure 3 is a block diagram of the elastic buffer. The receive clock "increments a receive side counter 40 so as to cause it to increment once for each 32 bit word. The receive side counter cycles through addresses 0, 1, 2, and 3 as it increments corresponding to activation of a chip select signal on lines 42, 44, 46 and 48, sequentially" (paragraph [0025]). That is, a *receive address* is generated after the reception of data. The counter then supplies this address (which may be a 0, 1, 2, or 3) to insertion/deletion logic 52 "for the purposes of detecting clock slip" (paragraph [0026]). Each of the addresses corresponds to one of the data registers. Logic 52 also receives a *transmit address* that is generated by a transmit side counter 54 which cycles between addresses 0, 1, 2, and 3 on every cycle of the transmit clock.

The logic 52 compares the receive address with the transmit address to determine if it is necessary to insert or remove primitives into one or more of data registers based on

the number of data registers (in this case, there are 4 data registers) within the elastic buffer and based on the distance between the receive address and the transmit address (in this case, the distance should be two) (paragraph [0029]). The logic 52 "compares the transmit and receive addresses at all times" (paragraph [0033]). Should the comparison determine a distance greater or less than two, the logic will add or delete a primitive into one of the data registers.

Insertion or deletion of a primitive causes the transmit counter 54 either to skip through one or more of the addresses 0, 1, 2, 3 or to count one or more of the addresses 0, 1, 2, 3 during the cycle. For example, during comparison of a receive address and a transmit address, it is determined that the distance is greater than two. Logic 52 activates a signal "Delete 1" that tells the transmit side counter 54 to skip the address of the data register that contains the primitive. Therefore, if the primitive is within the data register than corresponds to address 2, the counter 54 will increment as follows: 0, 1, 3, 0, 1, 2, 3... Skipping one of the addresses will realign each of the data registers to an earlier data line, and the distance of two between the receive and transmit addresses will go back to two, the optimal distance. (paragraph [0034]).

Independent claims 1, 17 and 27

Independent claim 1 is directed to a method in a receiving device for compensating for differences in clock frequencies between a transmitting device and a receiving device, comprising "identifying variable length groups of bits from the received stream along with an indication of whether the number of bits in the group represents an overrun or an underrun of bits" and "tracking whether an overrun or underrun criterion is satisfied based on the identified variable length group of bits."

Therefore, in contrast to Richmond, claim 1 describes a method where the number of bits received by a receiving device indicates an overrun or underrun condition. By way of an example, the specification at paragraph [00168] describes such a condition:

> Figure 45 is a state diagram of the symbol pointer tracker in one embodiment. The symbol pointer tracker tracks the start position of a symbol (e.g., frame) based on the start position of a synchronization symbol and the valid bits (e.g., V[8:9]) provided by the sampler. The symbol pointer tracker enters an initial state ("INIT") whenever the LD signal of the sync and null detector indicates that a synchronization symbol has been detected. The tracker stays in that initial state so long as the frame aligner is provided with 9 valid bits (i.e., N valid bits) at a time (i.e., V[8:9]="10" a normal condition). If the frame aligner is provided with 10 valid bits (i.e., V[8:9]="11" an overrun condition), then the tracker enters a first overrun state ("OVR1"), which means that the transmitter's clock frequency is faster than the receiver's clock frequency.

Therefore, the method of claim 1 relies on the number of bits in determining an overrun or underrun criterion. This number can be variable (for example, in the above paragraph, the frame aligner receiving 8 bits would signify and underrun condition and indicate that the transmitter's clock was slower than the receiver's clock). Moreover, the method of claim 1 does not rely on the transmission of a transmit clock.

As shown above, Richmond does not look to the number of groups of bits in a received stream in order to determiner an overrun or underrun condition. Additionally, there is no discussion of the system of Richmond identifying an indication of whether the number of bits in the groups represents and overrun or underrun of bits. On the other hand, Richmond compares addresses and seeks to maintain an optimal distance between the addresses. Therefore, for at least the above reasons, Richmond cannot anticipate claim 1, as it does not teach each and every element of the claim.

Independent claims 17 and 27 (and all the dependent claims) recite similar elements to claim 1, and therefore are patentable for at least the reasons stated with respect to claim 1. Moreover, the claims recite a novel combination of elements that is neither taught not suggested by the relied-upon references.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance and respectfully requests its early allowance.

Applicant submits herewith the extension of time fee and believes no additional fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 594728802US from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____

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